B2

While numerous circuits may be employed for driver 14 in the digital signal processing mode, an exemplary circuit 14A is shown in Fig. 3. The input signal applied to port 12 is supplied to an odd number of inverters 82-1 through 82-N (three inverters may suffice), as well as to one input of each of NOR-gate 84 and AND gate 86, as well as to pulse generator 88. (Pulse generator 88 is optional and its use is described in the incorporated patent . A second input of each of gates 84 and 86 is supplied from the output of the inverter string 82-1 through 82-N. The output of NOR-gate 84 supplies the DRIVEA signal on line 16 to coil L1 and the output of AND GATE 86 supplies the DRIVEB signal on line 18 to coil L2.

On page 7, replace the paragraph at lines 8 – 16 with the following:

B3

The operation of the circuit of Fig. 3 is now explained with reference to the waveforms of Fig. 4. The input signal again is assumed to be a logic signal which is high between times T1 and T2. The delayed and inverted state of the input signal which appears at node 92, termed D-I INPUT, thus is a copy of the input signal, inverted and delayed by the propagation delay of the inverter chain 82-1 through 82-N, which delay is labeled in the drawing as Δt. It is assumed that Δt is much smaller than the interval from T1 through T2. For example, Δt is typically just a few nanoseconds. The output from NOR-gate 84 consequently is high except during interval from T2 to T2 + Δt; and the output of the AND gate 86, the DRIVEB signal, is high except in the interval from T1 to T1+ Δt.

On page ~~11~~ 7, replace the paragraph at lines 17 – 21 with the following:

A diagrammatic illustration, as shown in Fig. 5, is useful to illustrate conceptually how such an isolator may be fabricated monolithically. Such fabrication may occur with the driver on a first substrate, SUB 1, and with the coils, Faraday shield, MR sensor and receiver on a second substrate, SUB 2, or with the entire apparatus on a single substrate (i.e., where SUB 1 and SUB 2 are the same substrate), as more fully explained below.

On page 7, replace the paragraph at lines 22-31 with the following:

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Without indicating any patterning, Fig. 6 shows a schematic side view of the layers of materials that form monolithically the coils, Faraday shield, sensor and receiver of Fig. 5. The resistive sensors 110 are formed on or in a semiconductor substrate 112 along with the receiver circuitry indicated generally in area 114. A thin layer of oxide 116 is then formed over the substrate. This is followed by a metallization layer 117 which connects to the substrate (i.e., the input's ground) and which provides the Faraday shield; appropriate positioning and area considerations are discussed below). A thick oxide layer 118 is applied over the metallization. On top of the thick oxide layer 118 there is formed a metallization layer 120 which is patterned to form coil L1 and L2 in appropriate geometric relationship and placement over sensor elements 110.

On page 10, replace the paragraph at lines 3-21 with the following:

B4

Referring to Figs. 11 and 12, there is shown a block diagram/diagrammatic illustration for an exemplary coil-coil isolator according to the invention. A driver circuit 172 on a first substrate 174 receives a logic signal input on pad 176 (referenced to an input ground pad 178). In the driver circuit, the input signal drives a Schmidt trigger 182 which, in turn, drives the enable inputs of a first pulse generator 184 and a second pulse generator 186, the former via an inverter 188. Information is coupled from the input side of the isolation barrier to the output side of the isolation barrier in the form of SET and RESET pulses to a differential receiver with hysteresis (not shown) connected to receive the outputs of coil windings 192, 194, which form the secondary windings of a transformer. The pulse generators 184, 186 drive (via wires 196-198) coils 202, 204, respectively, which form the primary windings of the transformer. Coils 202, 204, 192, 194 are formed on (which could include in) a second substrate 206 (which is electrically isolated from the first substrate). Between coils 202, 204 on one hand and coils 192, 194 on the other hand is formed an isolation layer 208 of a dielectric material. Preferably, a Faraday shield 210 also is formed between the primary and secondary windings, with the Faraday shield being connected to a ground 211 which is galvanically isolated from the input ground 178 and which is the reference ground for the output circuits (not shown) driven by coils